What is claimed is:

1. A customizable computing system, the system comprising:

a microprocessor;

a programmable logic device coupled to the microprocessor via a dedicated bus, and wherein the programmable logic device includes a configuration to provide I/O functionality to the system and includes one or more I/O interfaces; and

a system port coupled to the programmable logic device.

2. A system according to claim 1, further comprising a second bus coupled to the programmable logic device, wherein the system port is coupled to the second bus.

3. A system according to claim 1, further comprising a plurality of ports coupled to the programmable logic device.

4. A system according to claim 2, further comprising a plurality of ports coupled to the second bus.

5. A system according claim 1, wherein the programmable logic device includes a configuration to serve as a bridge between the dedicated bus and the system port.

6. A system according 2, wherein the programmable logic device includes a configuration to serve as a bridge between the dedicated bus and the second bus.

7. A system according to claim 1, wherein the microprocessor is a specific type and the programmable logic device includes a includes a configuration that provides functionality specific for the specific type of microprocessor.

8. A system according to claim 1, wherein the microprocessor is a specific type and the programmable logic device includes a includes a configuration that provides functionality that is independent of the specific type of microprocessor.

9. A system according to claim 8, wherein the microprocessor is a specific type and the programmable logic device includes a includes a configuration that provides functionality that is dependent on the specific type of microprocessor.

10. A system according to claim 9, wherein the programmable logic device includes a configuration to serve as a bridge between the functionality that that is independent of the specific type of microprocessor and the functionality that is specific for the specific type of microprocessor.

11. A system according to claim 1, wherein the programmable logic device is a field programmable gate array.

12. A system according to claim 1, wherein the microprocessor is of a type employing a RISC instruction set, such instruction set being at least 32 bits wide.

13. A system according to claim 1, wherein the microprocessor and the programmable logic device are integrated in the same physical package.

14. A system according to claim 1, wherein the dedicated bus includes a data path that is 64 bits wide.

15. A system according to claim 1, wherein the microprocessor has an architecture permitting pipeline processing of at least four simultaneously outstanding operations and the dedicated bus and programmable logic device are configured to support such pipeline processing.

16. A system according to claim 1, further comprising random access memory of at least 64 megabytes coupled to the microprocessor and wherein the microprocessor is of a type permitting operation of at least 500 MIPS and the system has a fully operational performance-to-power ratio of at least 300 MIPS per watt.

17. A system according to claim 12, wherein the microprocessor utilizes ARM architecture.

18. A system according to claim 17, wherein the microprocessor provides performance at least equal to that of an Intel Xscale 80200 model microprocessor.

19. A system according to claim 1, wherein the programmable logic device includes a configuration to provide a hardware video display driver.

20. A system according to claim 19, the system further includes random access memory coupled to the microprocessor and the video display driver shares the memory with the microprocessor.

21. A system according to claim 1, the system further includes random access memory coupled to the microprocessor and accessible over the dedicated bus.

22. A system according to claim 20, wherein the random access memory is accessible over the dedicated bus.